ABSTRACT OF THE DISCLOSURE

A semiconductor memory device has a semiconductor substrate, a first semiconductor region of a first conduction type formed on the semiconductor substrate, a second semiconductor region of a second conduction type opposite to the first conduction type, formed on the first semiconductor region. A trench capacitors having a trench extends through the first semiconductor region and the second semiconductor region, and is formed such that its top does not reach a top surface of the second semiconductor region, and the trench is formed therein with a conductive trench fill. A pair of gate electrodes is formed on the second semiconductor region, overlying the trench capacitor. A pair of insulating layers is formed to cover each of the pair of gate electrodes. A conductive layer is formed between the pair of insulating layers to self-align to each of the pair of insulating layers. The conductive layer has a leading end insulated from the second semiconductor region and reaching the interior of the second semiconductor region, and electrically connected to the conductive trench fill of the trench capacitor. A pair of third semiconductor regions of the first conduction type are formed in the second semiconductor region, and positioned opposite to each other with respect to the conductive layer. Each of the third semiconductor regions is directly in contact with the

conductive layer, and constitutes either a source or a drain of transistors having one of the pair of gate electrodes, respectively. The pair of third semiconductor regions is formed substantially to a uniform depth.